IN THE CLAIMS

Please cancel claims 14 through 19. Please amend claims 1 through 13 as follows.

1. **(PRESENTLY AMENDED)** A Quadrature Digital Waveform Synthesizer (QDWS) apparatus capable of correcting local oscillator (LO) leakage in a radar system, comprising:~~A Quadrature Error Corrected Digital Waveform Synthesizer (QECDWS) associated with a synthetic aperture radar (SAR), comprising:~~

~~a dual accumulator, including frequency and phase, to generate the necessary quadratic phase term (ϕ_i); and~~

~~a PEC RAM addressed by the instantaneous frequency (fi) output of the dual accumulator.~~

a complex bitstream, comprising an in-phase bitstream and a quadrature-phase bitstream;

a first pseudo-random noise dither generator output;

a second pseudo-random noise dither generator output;

a precision in-phase DC bias, comprising an effective precision;

a precision quadrature-phase DC bias, comprising an effective precision;

a complex waveform, comprising a in-phase (I) waveform and a quadrature-phase (Q) waveform; and

a radio frequency (RF) transmission of the radar system, wherein the RF transmission contains an LO leakage component.

2. **(PRESENTLY AMENDED)** The apparatus of claim 1 wherein the LO leakage is corrected in the RF transmission of the radar system.~~The invention of claim 1 further comprising a built-in loop capability, wherein inclusion of the built in loop allows the system to be calibrated to mitigate the non linear phase contributions of the SAR.~~

3. **(PRESENTLY AMENDED)** The apparatus of claim 2 wherein the LO leakage is consistently suppressed to at least -75 dBc.~~The invention of claim 2 wherein the effect on a fine-resolution SAR is to sharpen impulse response of the radar to maximize effective resolution capability and optimize image quality in the range dimension.~~

4. **(PRESENTLY AMENDED)** The apparatus of claim 1 wherein the first pseudo-random noise dither generator output is uniformly distributed, and the second pseudo-random noise dither generator output is uniformly distributed.~~The invention of claim 1 wherein quadrature amplitude and phase errors are compensated for with correction coefficients stored in a Quadrature Error Correction (QEC) RAM including a RAM for phase and a RAM for magnitude, wherein the QEC phase RAM output is added to the instantaneous phase of a cosine branch of a SINE/COSINE ROM.~~

5. **(PRESENTLY AMENDED)** The apparatus of claim 1 further comprising a first adder, comprising a plurality of inputs and an output, and an in-phase DC offset word, comprising a number of bits, wherein the first pseudo-random noise dither generator output is applied to a first input of the first adder and the in-phase DC offset word is applied to a second input of the first adder to produce the precision in-phase DC bias at the first adder output; and further comprising a second adder, comprising a plurality of inputs and an output, and a quadrature-phase DC offset word, comprising a number of bits, wherein the second pseudo-random noise dither generator output is applied to a first input of the second adder and the quadrature-phase DC offset word is applied to a second input of the second adder to produce the precision quadrature-phase DC bias at the second adder output.~~The invention of claim 4, wherein amplitude correction from the QEC magnitude RAM is applied to one of two multipliers located at each of the sine and cosine ROM outputs, wherein a determination as to which multiplier~~

~~is "active" is based on the sign of the twos compliment output of the QEC-MAG RAM.~~

6. **(PRESENTLY AMENDED)** The apparatus of claim 5 further comprising a third adder, comprising a plurality of inputs and an output, wherein the precision in-phase DC bias is applied to a first input of the third adder and the in-phase bitstream is applied to a second input of the third adder to produce a compensated in-phase bitstream at the third adder output; and further comprising a fourth adder, comprising a plurality of inputs and an output, wherein the precision quadrature-phase DC bias is applied to a first input of the fourth adder and the quadrature-phase bitstream is applied to a second input of the fourth adder to produce a compensated quadrature-phase bitstream at the fourth adder output.~~The invention of claim 5 further comprising a pseudo random noise dither generator, wherein problematic upconverter local oscillator (LO) leakage correctable when precision DC offsets are applied over the chirped pulse using a pseudo-random noise dither.~~

7. **(PRESENTLY AMENDED)** The apparatus of claim 6 further comprising an in-phase digital-to-analog converter (DAC), comprising a plurality of inputs, an output, and an instantaneous precision, wherein the compensated in-phase bitstream is applied to a first input of the in-phase DAC and the in-phase waveform of the complex waveform is produced at the in-phase DAC output; and further comprising a quadrature-phase DAC, comprising a plurality of inputs, an output, and an instantaneous precision, wherein the compensated quadrature-phase bitstream is applied to a first input of the quadrature-phase DAC and the quadrature-phase waveform of the complex waveform is produced at the quadrature-phase DAC output.~~A Quadrature Error Corrected Digital Waveform Synthesizer (QECDWS) associated with a synthetic aperture radar (SAR), comprising:~~

~~a dual accumulator, including frequency and phase, to generate the necessary quadratic phase term (□i);~~

~~a PEC RAM addressed by the instantaneous frequency (fi) output of the dual accumulator; and~~

~~a built-in loop, wherein inclusion of the built-in loop allows the system to be calibrated to mitigate the non-linear phase contributions of the SAR.~~

8. **(PRESENTLY AMENDED)** The apparatus of claim 7 wherein the LO leakage is corrected in the RF transmission of the radar system.~~The invention of claim 7 wherein the effect of the dual accumulator and PEC RAM is sharpened radar impulse response through maximized effective resolution capability and optimized image quality in the range dimension.~~

9. **(PRESENTLY AMENDED)** The apparatus of claim 8 wherein the LO leakage is consistently suppressed to at least -75 dBc.~~The invention of claim 7 wherein quadrature amplitude and phase errors are compensated for with correction coefficients stored in a Quadrature Error Correction (QEC) RAM including a RAM for phase and a RAM for magnitude, wherein the QEC phase RAM output is added to the instantaneous phase of a cosine branch of a SINE/COSINE ROM.~~

10. **(PRESENTLY AMENDED)** The apparatus of claim 7 wherein the effective precision of the precision in-phase DC bias is greater than the instantaneous precision of the in-phase DAC, and the effective precision of the precision quadrature-phase DC bias is greater than the instantaneous precision of the quadrature-phase DAC.~~The invention of claim 9, wherein amplitude correction from the QEC magnitude RAM is applied to one of two multipliers located at each of the sine and cosine ROM outputs, wherein a determination as to which multiplier is "active" is based on the sign of the twos compliment output of the QEC MAG RAM.~~

11. **(PRESENTLY AMENDED)** The apparatus of claim 7 further comprising a first noise sequence, comprising a number of bits, and a first pseudo-random

noise dither generator, comprising an input and the output, wherein the first noise sequence is applied to the input of the first pseudo-random noise dither generator.~~The invention of claim 7 further comprising a pseudo-random noise dither generator, wherein problematic upconverter local oscillator (LO) leakage correctable when precision DC offsets are applied over the chirped pulse using a pseudo-random noise dither.~~

12. **(PRESENTLY AMENDED)** The apparatus of claim 11 further comprising a second noise sequence, comprising a number of bits, and a second pseudo-random noise dither generator, comprising an input and the output, wherein the second noise sequence is applied to the input of the second pseudo-random noise dither generator.~~A method for correcting phase errors associated with synthetic aperture radar (SAR) systems using a Quadrature Error Corrected Digital Waveform Synthesizer (QECDWS), comprising:~~

~~utilizing frequency dependent phase error corrections to pre-distort phase characteristic of chirp associated with a radar system to compensate for frequency dependent phase nonlinearity of RF and microwave subsystems associate with the radar;~~

~~applying frequency dependent correction vectors to quadrature amplitude and phase of the radars systems synthesized output, wherein quadrature corrections cancel the radar system's quadrature upconverter errors to null the unwanted spectral image; and~~

~~generating an RF waveform having a theoretical chirp bandwidth equal to the QECDWS clock frequency of about 1 to 1.2 GHz with a high Spurious Free Dynamic Range (SFDR) necessary for high dynamic range radar systems such as a SAR.~~

13. **(PRESENTLY AMENDED)** The apparatus of claim 12 further comprising a Quadrature Error Correction (QEC) phase error correction random access memory (RAM); a Quadrature Error Correction (QEC) amplitude correction RAM; and a Phase Error Correction (PEC) RAM wherein a Quadrature Error Corrected

Digital Waveform Synthesizer (QECDWS) is formed, and wherein the QECDWS is capable of correcting problematic upconverter LO leakage when dithered precision DC biases are applied to bitstreams, and wherein the QECDWS is capable of correcting LO leakage, quadrature amplitude errors, and quadrature phase errors. ~~The method of claim 12, wherein problematic upconverter local oscillator (LO) leakage can be corrected by applying precision DC offsets over the chirped pulse using a pseudo-random noise dither, wherein a dither technique is used that can effectively produce a quadrature DC-bias including precision required to substantially suppress LO leakage.~~

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19. **(CANCELLED)**